REMARKS

Claims 1-29, all the claims pending in the application, stand rejected on prior art grounds. Applicants respectfully traverse these rejections based on the following discussion.

I. The Prior Art Rejections

Claims 1, 4-6, 8-11, 14-16, 18-21, 24-26, and 28-29 stand rejected under 35 U.S.C. §102(e) as being anticipated by Dutton et al. Claims 2-3, 7, 12-13, 17, 22-23, and 27 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Dutton et al. Applicants respectfully traverse these rejections based on the following discussion.

A. The Rejections Based on Dutton et al.

Applicants respectfully traverse these anticipation and obviousness rejections principally because Applicants feel that the Office Action misinterprets the language within the Dutton reference. More specifically, it is Applicants position that the Office Action improperly equates the buses shown in Figure 1 of Dutton with the channels within the inventive bridge. Because of this and other reasons, as explained in greater detail below, it is Applicants position that the claimed invention is not taught or suggested by Dutton.

In paragraph 5, the Office Action states that Dutton discloses "multiple buses (channels)," thereby indicating that there is no difference between the buses external to the bridge and channels within a bridge. However, Applicants submit that this interpretation is incorrect because independent claims 1, 10, and 20 explicitly distinguish between the channels of the bridge and the buses external to the bridge (e.g., independent claims 1, 10, and 20 explain that the channels of the bridge are connected to different buses, which requires that the channels and the buses must be different components). Further, the specification clearly explains the differences between channels within the

bridge and buses connected to the bridge (e.g., see Figure 2 illustrating buses connected to the bridge and Figure 3 illustrating channels within the bridge). In addition, the term "channels" is distinguished by those ordinarily skilled in this art field from the term "buses." Therefore, as detailed below, Applicants submit that by considering the buses to be channels, the Office Action ignores the explicit claim limitations and does not read the claims in light of the specification. These errors render the rejections improper.

With respect to the claim language distinguishing the channels from buses, independent claim 1 provides "a first channel dedicated to said processor local bus" and "a second channel dedicated to said peripheral device bus." Applicants submit that the language of independent claim 1 clearly provides that the channels are different from the buses because the structure defined by independent claim 1 includes one channel dedicated to the processor local bus and another channel dedicated to the peripheral device bus. Further, dependent claims 2-5 define that the channels includes buffer memories, random access memory, and a multiplexor. These claims further distinguish the claimed channels from buses because buses generally consist of conductors and not memories, multiplexors, etc. Thus, Applicants submit that independent claim 1 and its dependent claims clearly provide that the channels are not equivalent to buses.

Similarly, independent claim 10 defines that the structure includes "at least one bus connected to a unique dedicated channel in said bridge." This claim language provides that the channels are in the bridge and are therefore different than the buses shown in Figure 1 of Dutton that are external to the bridge. Further, this language of independent claim 10 also explains that the bus is connected to the channel, thereby again demonstrating that the channels are different structures from the buses. Once again, dependent claims 12-15 similarly define that the channels includes buffer memories, random access memory, and a multiplexor. These claims further distinguish the claimed channels from buses because buses generally consist of conductors and not memories, multiplexors, etc. Thus, Applicants submit that independent claim 10 and its dependent claims clearly provide that the channels are not equivalent to buses.

Also, independent claim 20 defines "a plurality of dedicated channels each uniquely connected to . . . at l ast one bus." As with the previously discussed

independent claims, this claim language of claim 20 indicates that the bus is connected to the channel, which logically requires that the channels be different structures than the buses. Again, the claims that depend from independent claim 20 add distinguishing features that further clarify that the channels and buses are different structures.

As mentioned above, the specification and drawings demonstrate that the channels are different structures from the buses. For example, Figure 2 illustrates many buses connected to the input/output interfaces of the bridge 230 and Figure 3 illustrates a number of buses (319-325) within the bridge. Further, page 7, lines 13-18 of the specification describe that each dedicated channel is uniquely connected to a different bus. Therefore, notwithstanding the claim language discussed above, when the claims are read in light of the specification, it is clear that the buses and channels are different devices.

Thus, it is Applicants position that the plain language of the claims and the specification defines that the channels are different structures than the buses. Therefore, the Office Action's interpretation that the buses and channels are equivalent is incorrect with respect to the structures defined by independent claims 1, 10, and 20. Further, if the channels are considered to be the same thing as buses, Dutton could not teach or suggest the claimed invention because a device cannot logically connect to itself. More importantly, because Dutton merely states that item 106 is a bridge (column 4, lines 15-32) without explaining any details of the bridge, Dutton cannot be said to teach or suggest different channels being dedicated to different exterior devices as defined by independent claims 1, 10, and 20.

Further, as demonstrated in the previous amendment filed by Applicants on July 30, 2003, the invention provides non-blocking communication through multiple reserved lanes in the bridge (e.g., channels 319-325) that are managed by an implicit protocol (e.g., buffers 314 and multiplexors 316). The invention avoids relying on handshaking signals that leads to blocking communications when a destination or a shared resource is overloaded. The virtual channel communication architecture (VCCA), shown in Applicants' Figures 2-4, provides application specific bus interface flow control, by coordinating the access of resource competing components using reserved lanes. The

virtual channel scheduler module uses multiple FIFO buffers 314, dedicated to distinct virtual channels 319-325, to allow the invention to implement the required multiple reserved lanes. With the invention, transactions occurring on each port interface may be routed to adjacent ports without having to pass through a bus. Similarly, each port has a data-path dedicated to the processor local bus 206.

To the contrary, Dutton merely describes a conventional bridge 106 and does not explain any details about the bridge 106. More specifically, in column 4, lines 15-48, Dutton describes that the chipset logic 106 includes various bridge logic and includes arbitration logic 107. The chipset logic 106 is similar to the Triton chipset available from Intel Corporation, including certain arbiter modifications to accommodate the real-time bus of the present invention. A second level or L2 cache memory may be coupled to a cache controller in the chipset logic 106, as desired. The bridge or chipset logic 106 couples through a memory bus 108 to main memory 110. The chipset logic 106 includes a memory controller for interfacing to the main memory 110 and also includes the arbitration logic 107. The chipset logic 106 includes various peripherals, including an interrupt system, a real time clock (RTC) and timers, a direct memory access (DMA) system, and ROM/Flash memory. Other peripherals are comprised in the chipset logic 106, including communications ports, diagnostics ports, command/status registers, and non-volatile static random access memory (NVSRAM). The host/PCI/cache bridge or chipset logic 106 also interfaces to a local expansion bus or system bus 120.

The only discussion of different byte channels in Dutton relates to the multimedia devices 142-146. More specifically, in column 6, lines 10-31, Dutton describes the byte slicing logic that efficiently uses each data byte channel of the bus. However, this discussion only relates to the multimedia devices and does not relate to the bridge. To the contrary, there is no discussion in Dutton regarding the bridge 106 having multiple channels, much less each channel being uniquely dedicated to a different bus, memory unit, input/output unit, peripheral device, etc.

Therefore, it is Applicants position that Dutton does not teach any details regarding the bridge 106 and therefore does not teach or suggest that the "bridge includes a first channel dedicated to said processor local bus . . . a second channel dedicated to

said peripheral device bus . . . a third channel dedicated to said memory unit; and . . . a fourth channel dedicated to said input/output unit," as defined by independent claim 1; that the bus, memory unit, and input/output unit are each "connected to a uniquely dedicated channel in said bridge"; as defined by independent claim 10; or a bridge that has "dedicated channels each uniquely connected to one or more of:" the bus, memory unit, input/output unit, and peripheral device, as defined by independent claim 20 . Therefore, Applicants submit that independent claims 1, 10, and 20 are patentable over the prior art of record. Further, dependent claims 2-9, 11-19, and 21-29 are similarly patentable, not only by virtue of their dependency from a patentable independent claim, but also by virtue of the additional features of the invention defined. In view the foregoing, the Examiner is respectfully requested to reconsider and withdraw these rejections.

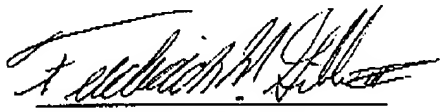
II. Formal Matters and Conclusion

In view of the foregoing, Applicants submit that claims 1-29, all the claims presently pending in the application, are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary.

Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0456.

Respectfully submitted,



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